



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,253	06/26/2002	Mike Ryken	8781-US-PA	8436

31561 7590 10/19/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
7 FLOOR-1, NO. 100  
ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER

TSAI, HENRY

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/064,253

Applicant(s)

RYKEN, MIKE

Examiner

Henry W.H. Tsai

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Art Unit: 2183

**DETAILED ACTION**

***Specification***

1. The disclosure is objected to because of the following informalities:

at page 7, line 4, "sill" should read -still-.

Appropriate correction is required.

***Claim Objections***

2. Claims 2 and 6 are objected to because of the following informalities:

In claim 2, line 1, "an" should read -a-. Similar problems exist in claim 6.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2183

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 3, "the storage space" lacks proper antecedent basis since it was not mentioned previously.

In claim 1, line 4, it is not clear what is meant by "the processor intends to enter the debug mode" since "intend" is an abstract term of a mental process. How to measure the "intend" in a processor is not well defined. Note an intention is not necessary to be executed. Similar problems exist in line 9.

In claim 1, line 5, it is not clear what is meant by "without need an actual track". Should it be changed to - without need of an actual track- ?

In claim 4, lines 1-2, it is not clear what is meant by "the data storage space is a new instruction address" since an address is a value which can not be defined to equivalent to a storage space.

In claim 5, lines 4-5, it is not clear what is meant by "when a debug mode is desired" since "desire" is an abstract term of a mental process. How to measure the "desire" in a

Art Unit: 2183

processor is not well defined. Note a desire is not necessary to be executed.

In claim 6, line 1, "the data storage space" lacks proper antecedent basis since it was not mentioned previously. Should it be changed to - the data storing space - ? Similar problems exist in claims 6-8.

In claim 9, line 2, it is not clear how a resume register functioning as saving device, can comprise many elements such as the first and second multiplexers and others. Similar problems exist in claim 11. The limitations of the claimed invention are not clear.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2183

6. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Stallings "Computer Organization and Architecture", 1996, Prentice-Hall, Inc., 4th edition, pp 190-193 (herein referred to as Stallings).

Referring to claim 1, Stallings discloses, as claimed, a method of saving/restoring a processor state after a processor entering/exiting an debug mode (the is the situation when the interrupt is for debugging), the method comprising: storing an address (N+1 in Program Counter, see Fig. 6.7(a)) of a resume instruction (the first instruction that is not executed due to the new mode change) into the data storage space (control stack in the main memory see Fig. 6.7 (a)), when the processor intends to enter the debug mode; performing a debugging instruction (the is the situation when the interrupt is for debugging) during the debug mode without need an actual track on the number of program counter (PC) for the debugging instruction being executed in the debug mode (the is the situation when the interrupt is for debugging); and fetching the address (N+1, see Fig. 6.7(b)) of the resume instruction from the data storage space (control stack in the main memory see Fig. 6.7(b)), when the processor intends to exit the debug mode.

Referring to claim 5, Stallings discloses, as claimed, a debugging method for a debugger associating with a processor; the method comprising: storing a program counter (PC) (N+1 in Program Counter, see Fig. 6.7(a)) of a processor state with respect to a resume instruction (the first instruction that is not executed due to the new mode change) into a data storing space (control stack in the main memory see Fig. 6.7(a)) in the debugger, when a debug mode (the is the situation when the interrupt is for debugging) is desired; performing a debugging instruction by the debugger during the debug mode (the is the situation when the interrupt is for debugging) without need of an actual track on the number of PC for the debugging instruction being executed in the debug mode; and fetching the PC (N+1, see Fig. 6.7(b)) of the resume instruction at the data storing space (control stack in the main memory see Fig. 6.7(b)) for the processor, when the debug mode is exited.

As to claims 2 and 6, Stallings also discloses: the data storage space is provided by a data storage device (control stack in the main memory see Fig. 6.7(a)).

As to claims 3 and 7, Stallings also discloses: the data storage space is provided by a register (control stack in the main memory see Fig. 6.7 (a)).

Art Unit: 2183

As to claims 4 and 8, Stallings also discloses: the data storage space is a new instruction address (control stack in the main memory see Fig. 6.7 (a) which can store a new address).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stallings in view of Sample (U.S. Patent Application No. 2002/0177990) (herein referred to as Sample'990).

Stallings discloses the claimed invention except for: a first flip-flop, receiving a program counter (PC) as the resume address, a control signal for entering a debug mode; a multiplexer, receiving the PC and the resume address from the first flip-flop, and a control signal for exiting the debug



Art Unit: 2183

mode; and a second flip-flop, receiving an output data of the multiplexer and exporting the PC.

Sample'990 discloses a system using a first flip-flop (2004, see Fig. 20c), a second flip-flop (2004, see Fig. 20c) and a multiplexer (2005, see Fig. 20c) for control the signal and data movement (for such as counter 2016, see Fig. 20c) in the processor.

Further, using a flip-flop to save a data in a memory device and using a multiplexer to select an output are well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Stallings's device to comprise a first flip-flop, receiving a program counter (PC) as the resume address, a control signal for entering a debug mode; a multiplexer, receiving the PC and the resume address from the first flip-flop, and a control signal for exiting the debug mode; and a second flip-flop, receiving an output data of the multiplexer and exporting the PC, as taught by Sample'990, in order to facilitate saving the data and selectively control the output data for the Stallings's system.

### ***Conclusion***

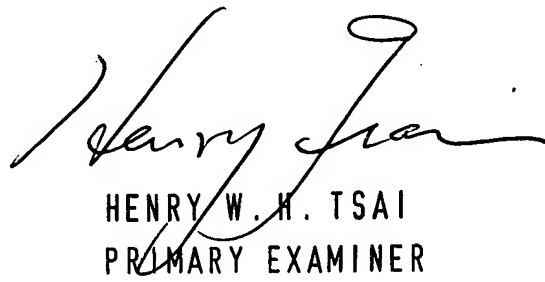
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Burgun et al.'553 discloses a microprocessor comprising a first flip-flop, a second flip-flop and a multiplexer for control the signal and data movement in the processor as shown in Fig. 18. Swoboda et al.'339 discloses an emulation suspension mode handling multiple stops and stars. As shown in Fig. 6, the processor also handles the debugging mode between the stop mode and real-time mode.

### ***Contact Information***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 receptionist whose telephone number is (703) 305-3900.

Art Unit: 2183

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306**. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI  
PRIMARY EXAMINER

October 18, 2004